Abstract

Address generator for generating addresses for testing a circuit

Address generator for generating addresses for testing an addressable circuit (2), having: at least one base address register (12) for buffer-storing a base address, the base address register (12) in each case being assigned an associated offset register group (13) having a plurality of offset registers for buffer-storing relative address values; a first multiplexer circuit (38), which, in a manner dependent on a base register selection control signal, switches through an address buffer-stored in the base address register (12) to a first input (59) of an addition circuit (60) and to an address bus (3), which is connected to the circuit (2) to be tested; a second multiplexer circuit (17), which, in a manner dependent on the base register selection control signal, through-connects the offset register group (13) associated with the through-connected base address register (12) to a third multiplexer circuit (25), which, in a manner dependent on an offset register selection control signal, through-connects an offset register of the through-connected offset register group (13) to a second input (61) of the addition circuit (60); the addition circuit (60) adding the address present at the first input to the relative address value present at the second input (61) to form an address which is buffer-stored in the base address register (12).

Figure 4